SSC8239GS1

P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-35V	±20V	6mR@-10V	-68A
		8mR@-4V5	

➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wild range of given voltage ratings(4.5V~25V) such as load switch and battery protection.

100% UIS Tested.

➢ Applications

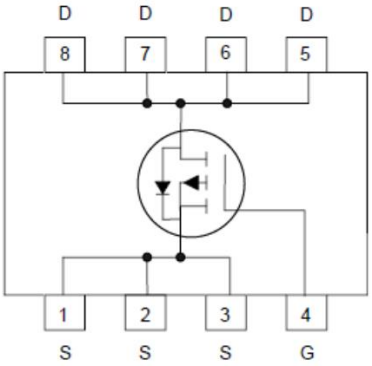
- Load Switch
- NB battery
- DCDC conversion

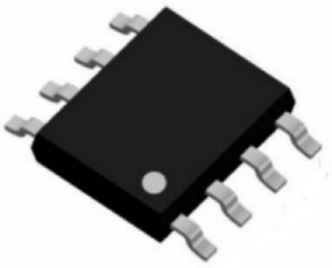
➢ Ordering Information

Device	Package	Shipping
SSC8239GS1	SOP8	4000/Reel

➢ Pin configuration

Top view





Bottom View

(Y: year/W: week)

Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-to-Source Voltage		-35	V
V_{GSS}	Gate-to-Source Voltage		±20	V
I_D	Continuous Drain Current [d]	TC=25℃	-68	A
		TC=100℃	-37	
I_{DSM}	Continuous Drain Current [a]	TA=25℃	-16	A
		TA=70℃	-11	
I_{DM}	Pulsed Drain Current [b]		-272	A
I_{AS}	Avalanche Current[b] L=0.5mH		-34	A
E_{AS}	Avalanche Energy[b] L=0.5mH		289	mJ
P_D	Power Dissipation [d]	TC=25℃	44	W
		TC=100℃	17	W
P_{DSM}	Power Dissipation [a]	TA=25℃	2.5	W
		TA=70℃	1.6	W
T_J	Operation junction temperature		-55 to 150	℃
T_{STG}	Storage temperature range		-55 to 150	

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	50	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance [c]	22	
	Junction-to-Case Thermal Resistance [d]	2.8	

Note:

a. The value of RθJA is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with TA=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

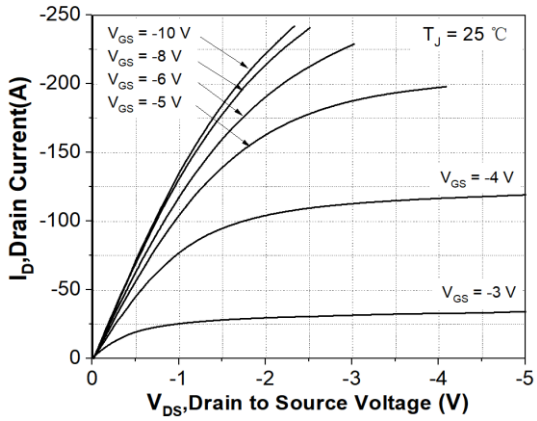
c. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

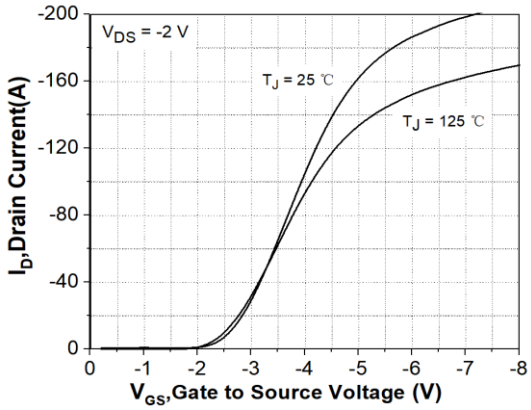
d. The value of $R_{\theta JC}$ has been determined of the temperature difference between junction and the case surface in contact with water cooled copper heat sink .

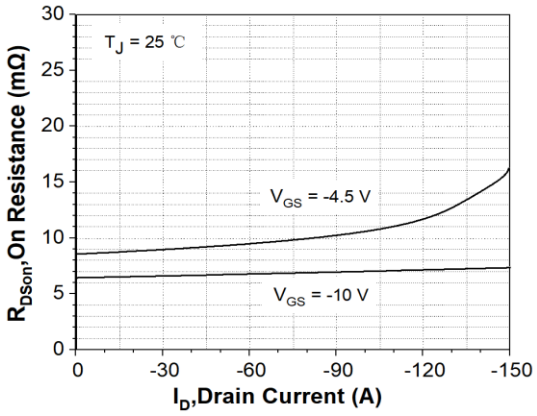
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

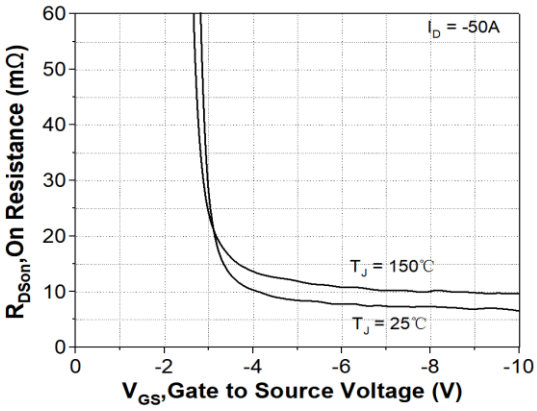
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V , ID=-250uA	-35			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS , ID=-250uA	-1	-1.4	-3	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-10V , ID=-15A		6	7.5	mR
		VGS=-4.5V , ID=-10A		8	10	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-30V , VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±20V , VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V , ID=-10A		11		S
V_{SD}	Forward Voltage	VGS=0V , IS=-10A		-0.8	-1.3	V
Ciss	Input Capacitance	VDS=-15V , VGS=0V, f=1MHz		4800		pF
Coss	Output Capacitance			510		
Crss	Reverse Transfer Capacitance			410		
Q_G	Total Gate charge	VGS=-10V , VDS=-15V, ID=-20A		80		nC
Q_{GS}	Gate to Source charge			10		
Q_{GD}	Gate to Drain charge			19		
$T_{D(ON)}$	Turn-on delay time	VGS=-10V, VDS=-15V, RL=0.75R, RG=3R		17		ns
Tr	Rise time			50		
$T_{D(OFF)}$	Turn-off delay time			110		
Tf	Fall time			25		
Trr	Diode Recovery Time	IF=-20A, di/dt=500A/us		25		ns
Qrr	Diode Recovery Charge			17		nC

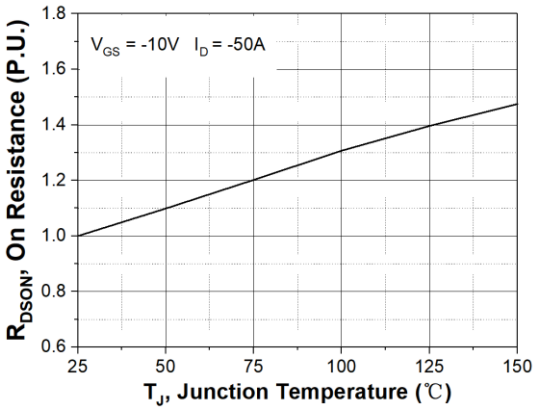
➢ Typical Characteristics(T_A=25℃ unless otherwise noted)

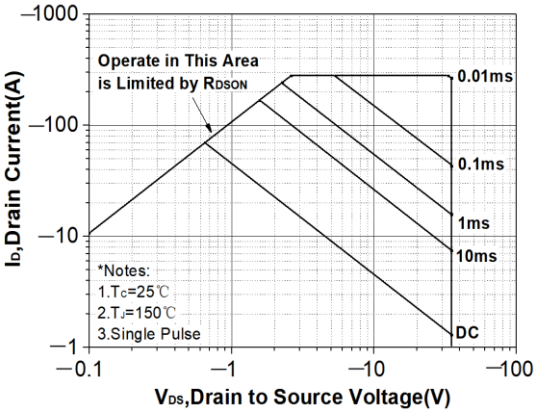


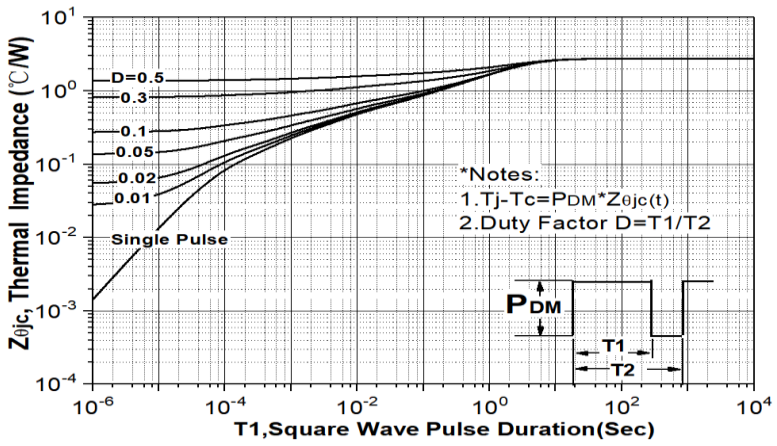




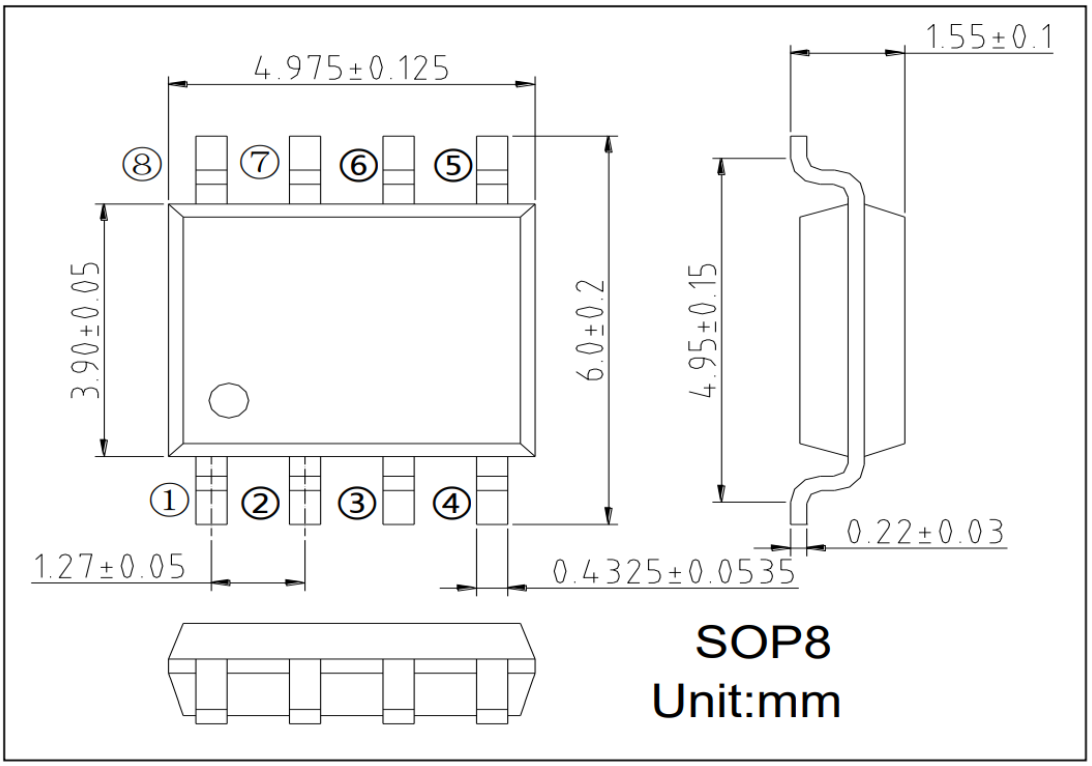








➢ Package Information



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