



SSC7002EGSD

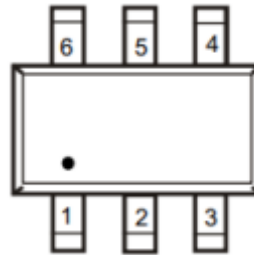
Dual N-Channel Enhancement Mode MOSFET

➤ Features

VDS	VGS	RDSON Typ.	ID	ESD
60V	±20V	2R@10V	0.3A	1KV
		3R@4V5		

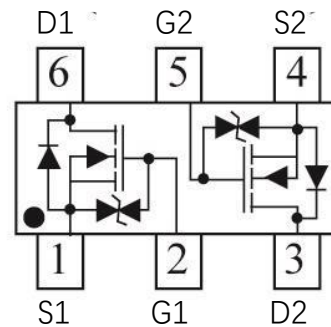
➤ Pin configuration

Top view



➤ Description

The SSC7002EGSD is dual N-channel enhancement MOS field effect transistor. With low on-resistance and fast switching speed. It is ideal for portable equipment with high saturation current capability and ESD protected.

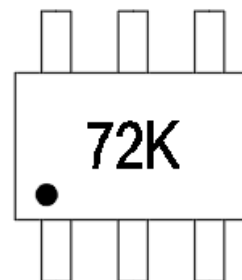


➤ Applications

- Voltage controlled small signal switch
- Direct Logic-Level Interface: TTL/CMOS
- Display, Memories, Transistors, etc.

➤ Ordering Information

Device	Package	Shipping
SSC7002EGSD	SOT363	3000/Reel



Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	60	V
V_{GSS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current ^a	0.3	A
I_{DM}	Pulsed Drain Current ^b	0.8	A
P_D	Power Dissipation ^c	0.45	W
P_{DSM}	Power Dissipation ^a	0.25	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		520	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		290	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $T_A=25^{\circ}\text{C}$.The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_J(\text{MAX})=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

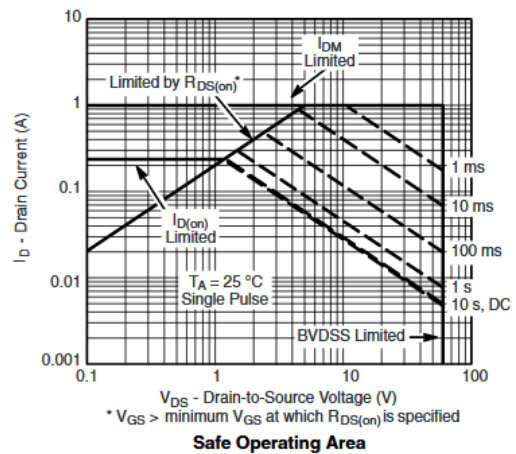
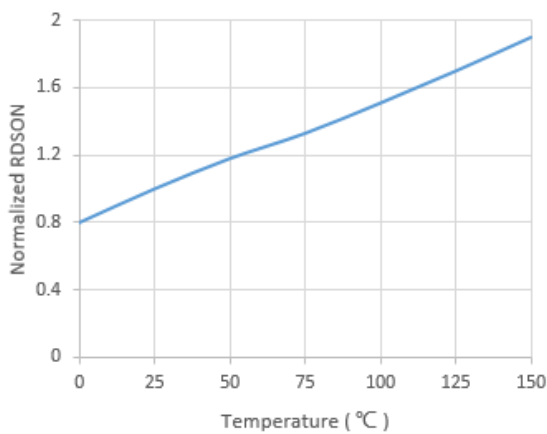
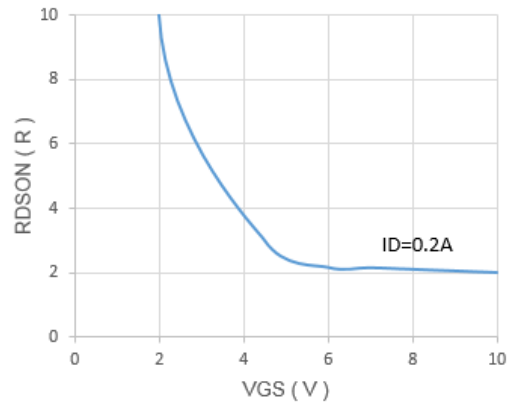
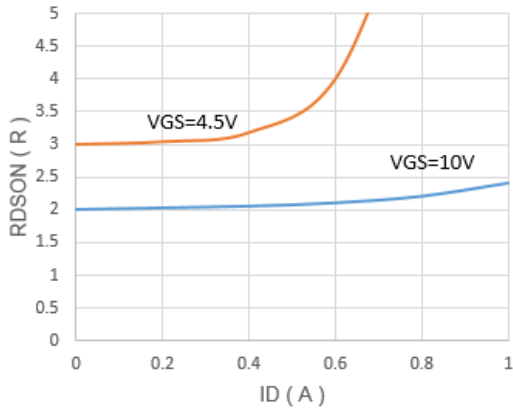
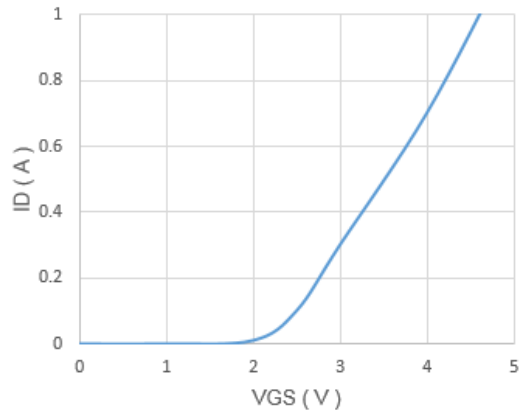
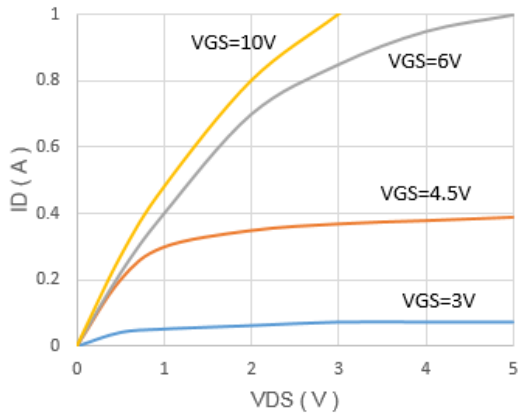


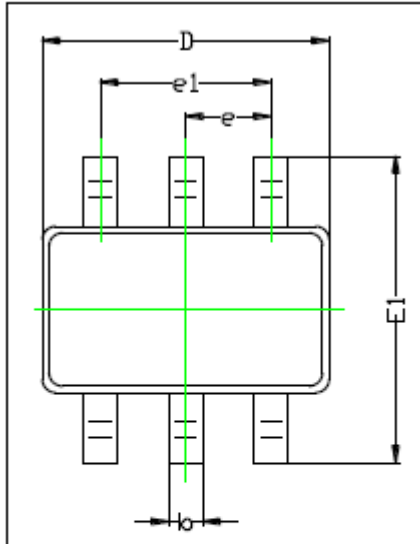
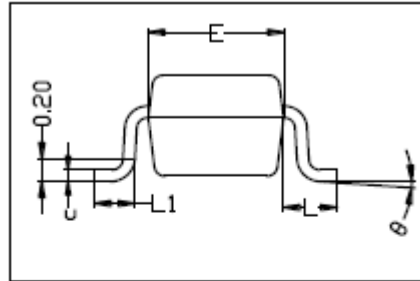
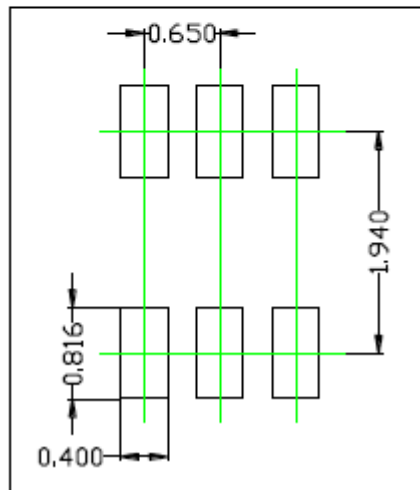
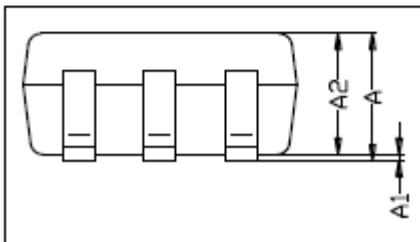
➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=1mA$	1		2.5	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=0.3A$		2	4	R
		$V_{GS}=4.5V, I_D=0.2A$		3	6	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=48V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 10	μA
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=0.3A$		0.8	1.5	V
G_{FS}	Transconductance	$V_{DS}=5V, I_D=0.3A$		0.4		S
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		40		pF
C_{oss}	Output Capacitance			30		
C_{rss}	Reverse Transfer Capacitance			10		
Q_g	Total Gate charge	$V_{GS}=10V, V_{DS}=30V, I_D=0.3A$		1.2		nC
Q_{gs}	Gate to Source charge			0.21		
Q_{gd}	Gate to Drain charge			0.12		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=10V, V_{DS}=50V, R_G=6R, R_L=250R$		7		ns
T_r	Rise time			5		
$T_{D(OFF)}$	Turn-off delay time			25		
T_f	Fall time			10		



➤ Typical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



➤ Package Information
TOP VIEW

SIDE VIEW

SOLDERING PATTERN

FRONT VIEW


SYMBOL	DIMENSIONS IN MILLIMETER	
	MIN	MAX
A	0.900	1.000
A1	0.000	0.100
A2	0.900	1.000
b	0.150	0.300
c	0.100	0.150
D	2.000	2.200
E	1.150	1.350
E1	2.150	2.400
e	0.650 TYP.	
e1	1.200	1.400
L	0.525 REF.	
L1	0.260	0.450
θ	0°	8°



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