



SSC8029GQ4

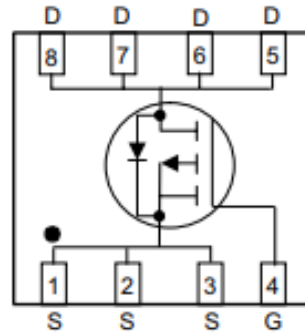
P-Channel Enhancement Mode MOSFET

➤ **Features**

VDS	VGS	RDS(on) Typ.	ID
-20V	±12V	17mR@-4V5	-15A
		21mR@-2V5	
		26mR@-1V8	

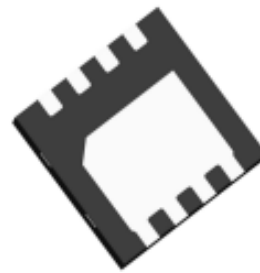
➤ **Pin configuration**

Top view



➤ **Description**

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wide range of given voltage ratings(4.5V~18V) such as load switch and battery protection.



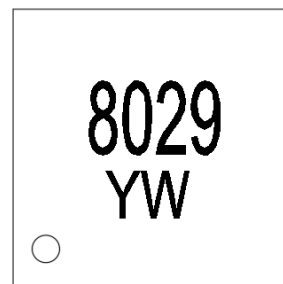
Bottom View

➤ **Applications**

- Load Switch
- NB battery
- DCDC conversion

➤ **Ordering Information**

Device	Package	Shipping
SSC8029GQ4	DFN3x3	5000/Reel



(Y: year/W: week)

Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^a	-15	A
I_{DM}	Pulsed Drain Current ^b	-45	A
P_D	Power Dissipation ^c	15	W
P_{DSM}	Power Dissipation ^a	2.5	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		60	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		9	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper,in a still air environment with $T_A=25^{\circ}\text{C}$.The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

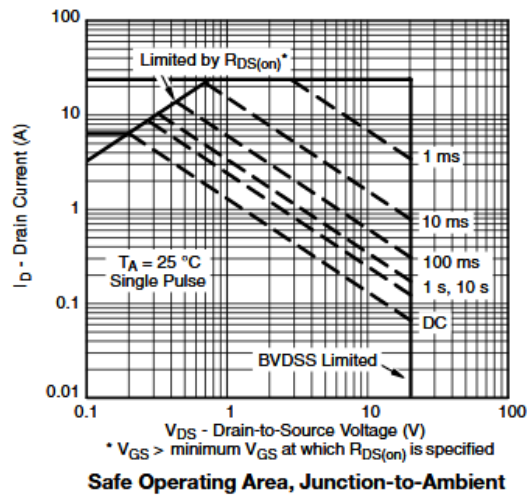
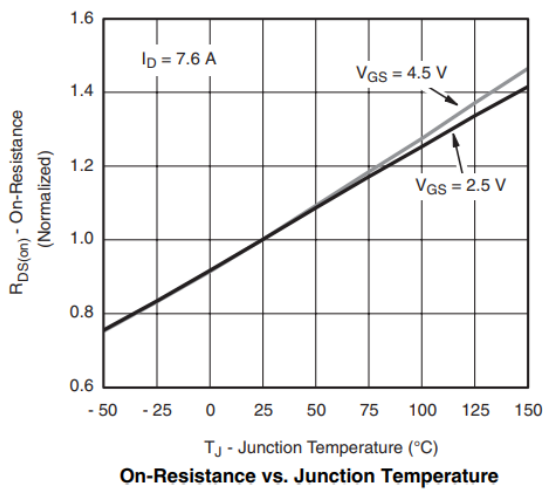
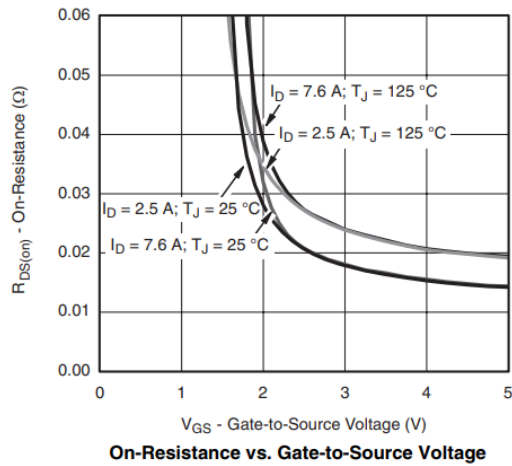
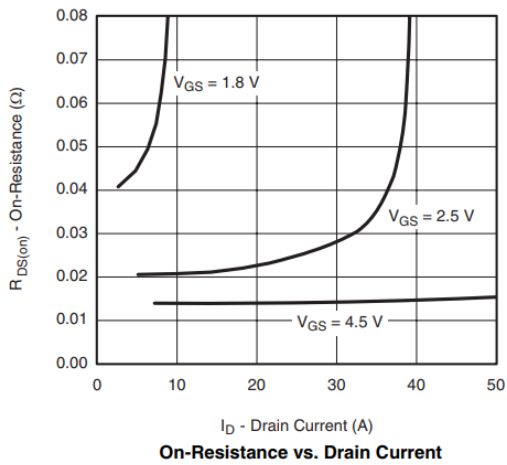
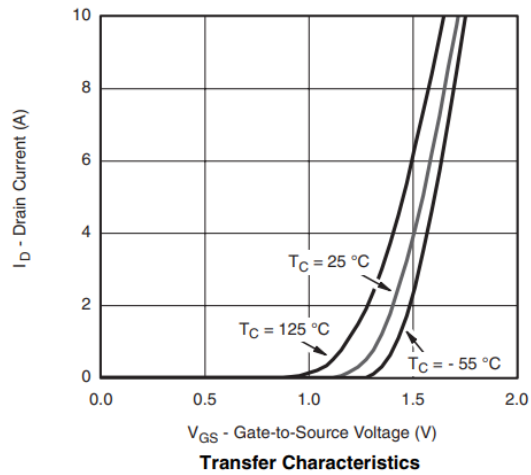
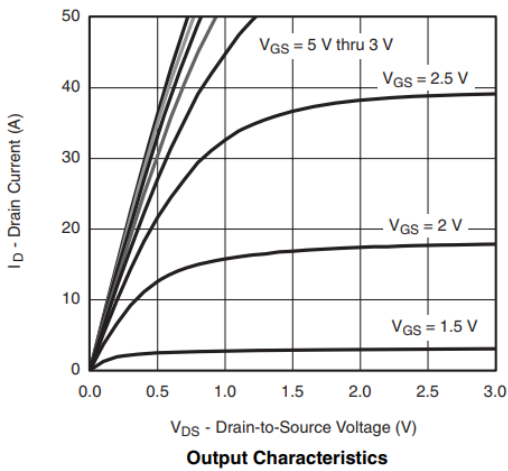


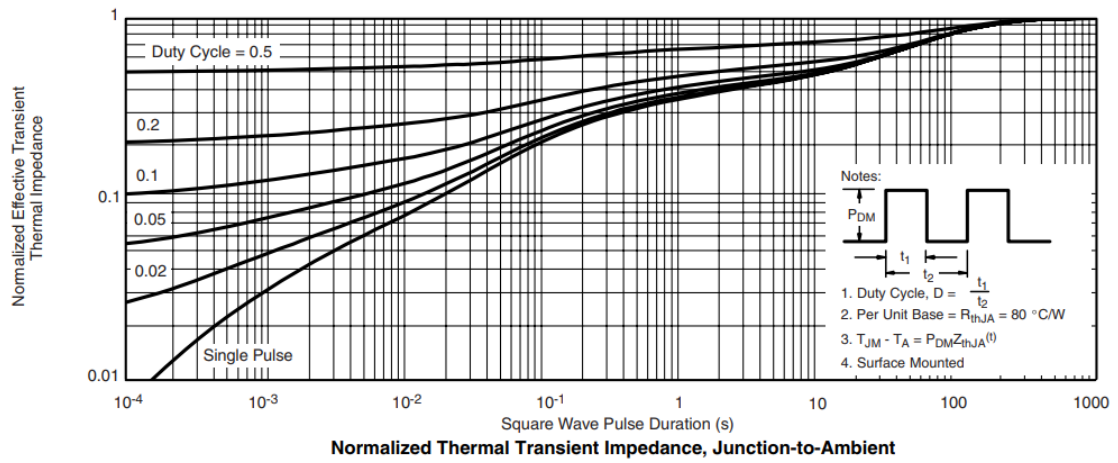
➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

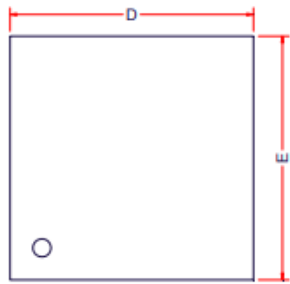
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5	-0.6	-1	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=-4.5V, I_D=-5.5A$		17	22	mR
		$V_{GS}=-2.5V, I_D=-2.5A$		21	27	
		$V_{GS}=-1.8V, I_D=-1.8A$		26	50	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$			-1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			± 100	nA
G_{FS}	Transconductance	$V_{DS}=-5V, I_D=-10A$		25		S
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=-1A$		-0.75	-1.3	V
C_{iss}	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$		1828		pF
C_{oss}	Output Capacitance			203		
C_{rss}	Reverse Transfer Capacitance			201		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-4.5V,$ $V_{DS}=-10V, R_L=6R, R_G=6R,$ $I_D=-6.5A$		16		ns
T_r	Rise time			14		
$T_{D(OFF)}$	Turn-off delay time			78		
T_f	Fall time			66		



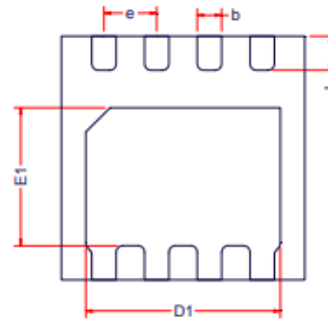
➤ **Typical Characteristics** ($T_A=25^\circ\text{C}$ unless otherwise noted)



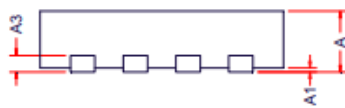


➤ Package Information


TOP VIEW



BOTTOM VIEW



SIDE VIEW

DFN3x3-8L

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.20Ref		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
b	0.25	0.30	0.35
e	0.65BSC		
L	0.37	0.42	0.47



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