



## SSC8035GS6

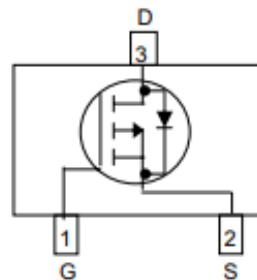
### P-Channel Enhancement Mode MOSFET

#### ➤ Features

VDS	VGS	RDS(on) Typ.	ID
-30V	±12V	51mR@-10V	-4A
		60mR@-4V5	
		98mR@-2V5	

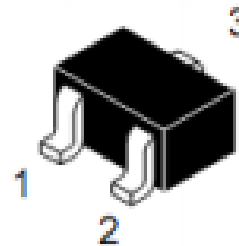
#### ➤ Pin configuration

Top view



#### ➤ Description

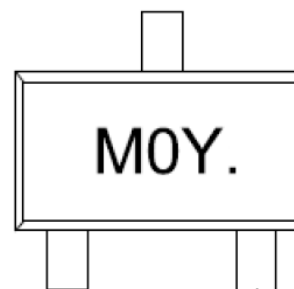
This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. Excellent thermal and electrical capabilities.



SOT23

#### ➤ Applications

- Load Switch
- Portable Devices
- DCDC conversion



Marking

#### ➤ Ordering Information

Device	Package	Shipping
SSC8035GS6	SOT23	3000/Reel



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	-30	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	-4	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	-17	A
$P_D$	Power Dissipation <sup>c</sup>	1.3	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.73	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		180	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		100	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(\text{MAX})}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

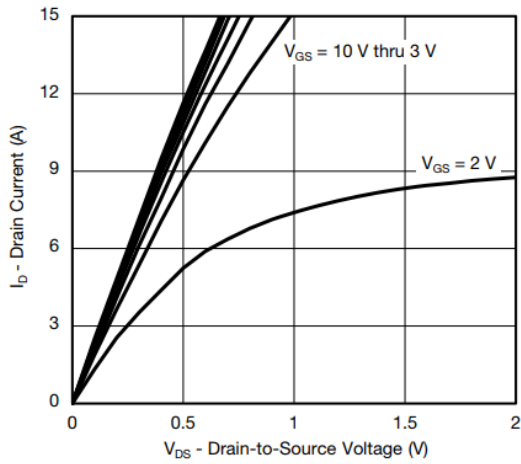


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

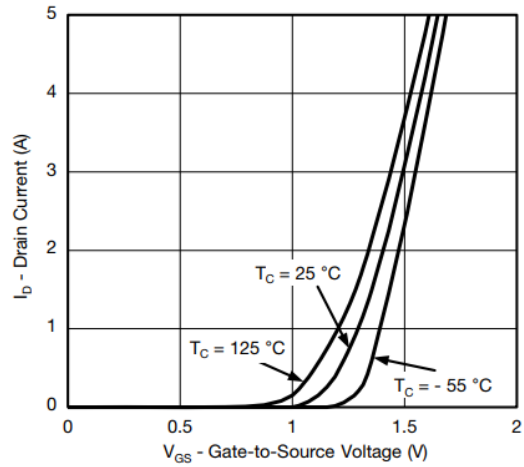
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.7	-1	-1.3	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=-10V, I_D=-4A$		51	65	mR
		$V_{GS}=-4.5V, I_D=-2A$		60	75	
		$V_{GS}=-2.5V, I_D=-1A$		98	120	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0V$			-1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=-5V, I_D=-3A$		10		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=-1A$		-0.78	-1	V
$C_{iss}$	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$		600		pF
$C_{oss}$	Output Capacitance			85		
$C_{rss}$	Reverse Transfer Capacitance			66		
$T_{D(ON)}$	Turn-on delay time			13		
$T_r$	Rise time	$V_{GS}=-10V,$ $V_{DS}=-15V, R_L=15R, R_G=6R,$ $I_D=-2.0A$		7		ns
$T_{D(OFF)}$	Turn-off delay time			40		
$T_f$	Fall time			10		



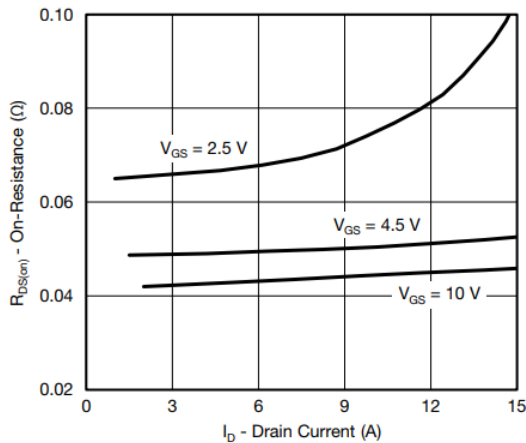
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)



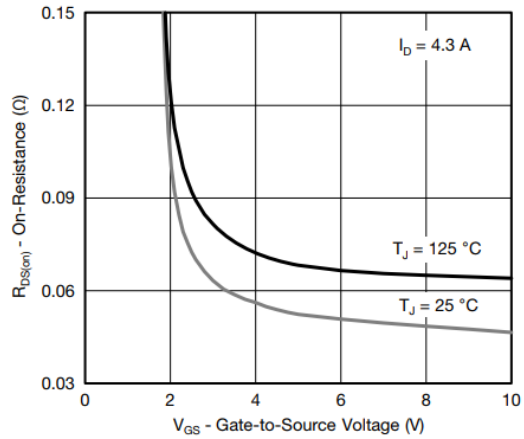
**Output Characteristics**



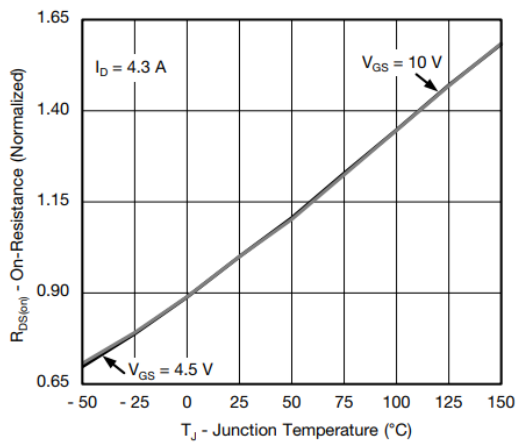
**Transfer Characteristics**



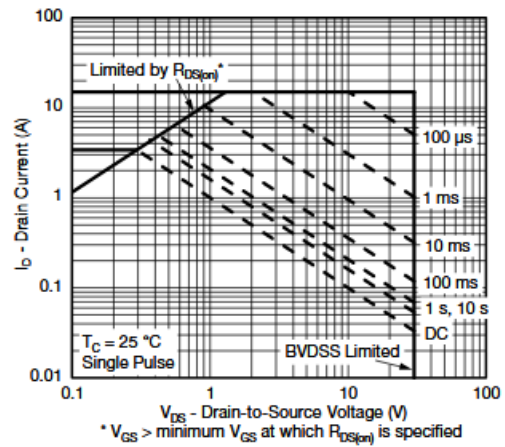
**On-Resistance vs. Drain Current**



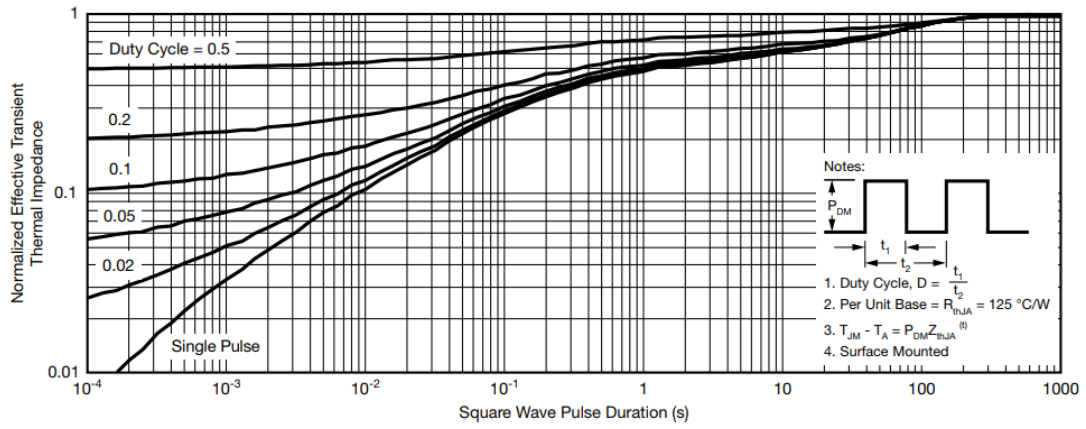
**On-Resistance vs. Gate-to-Source Voltage**



**On-Resistance vs. Junction Temperature**



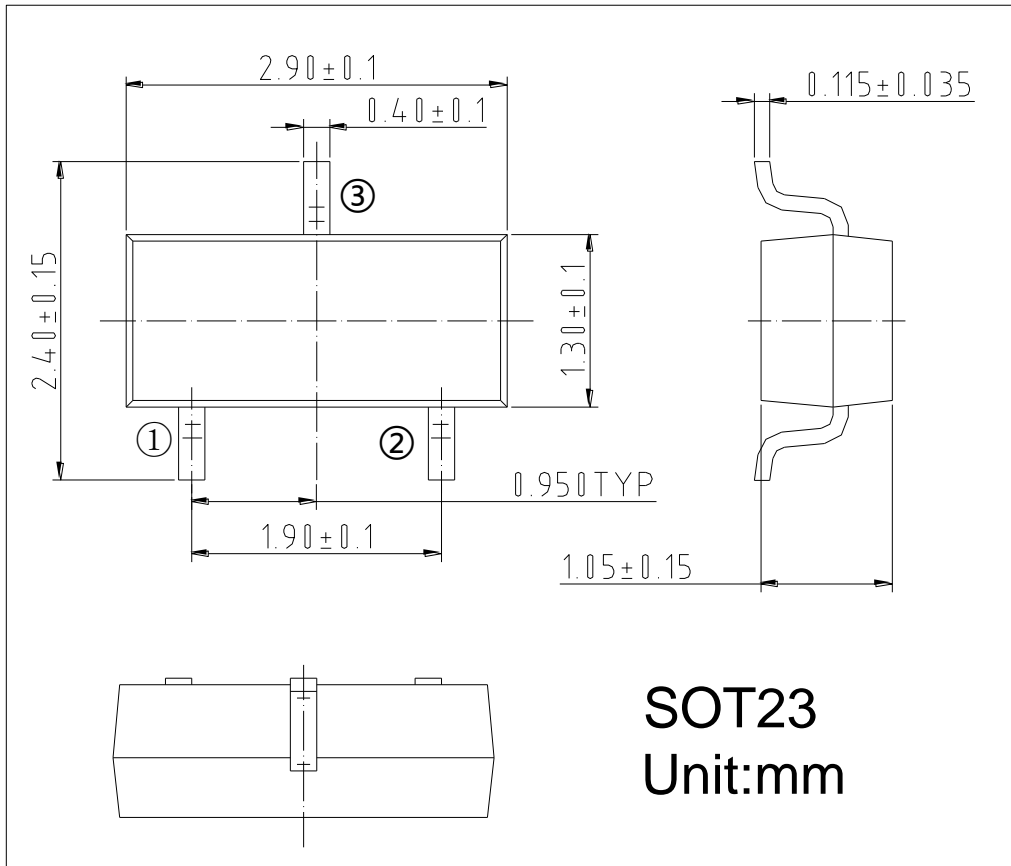
**Safe Operating Area, Junction-to-Ambient**



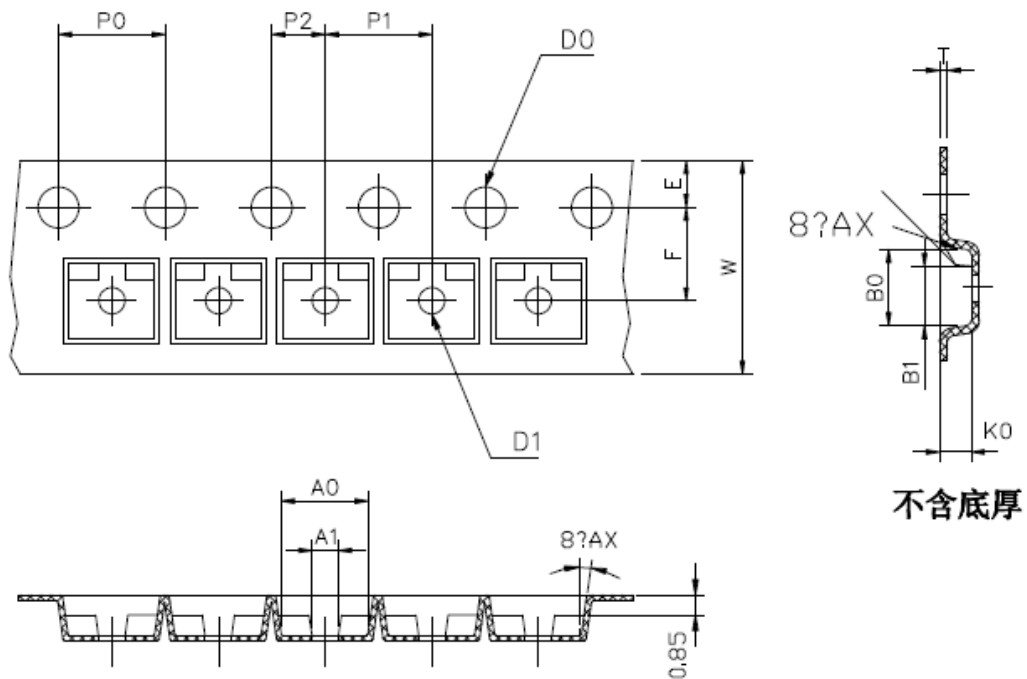
Normalized Thermal Transient Impedance, Junction-to-Ambient



➤ Package Information



TAPE AND REEL DATA

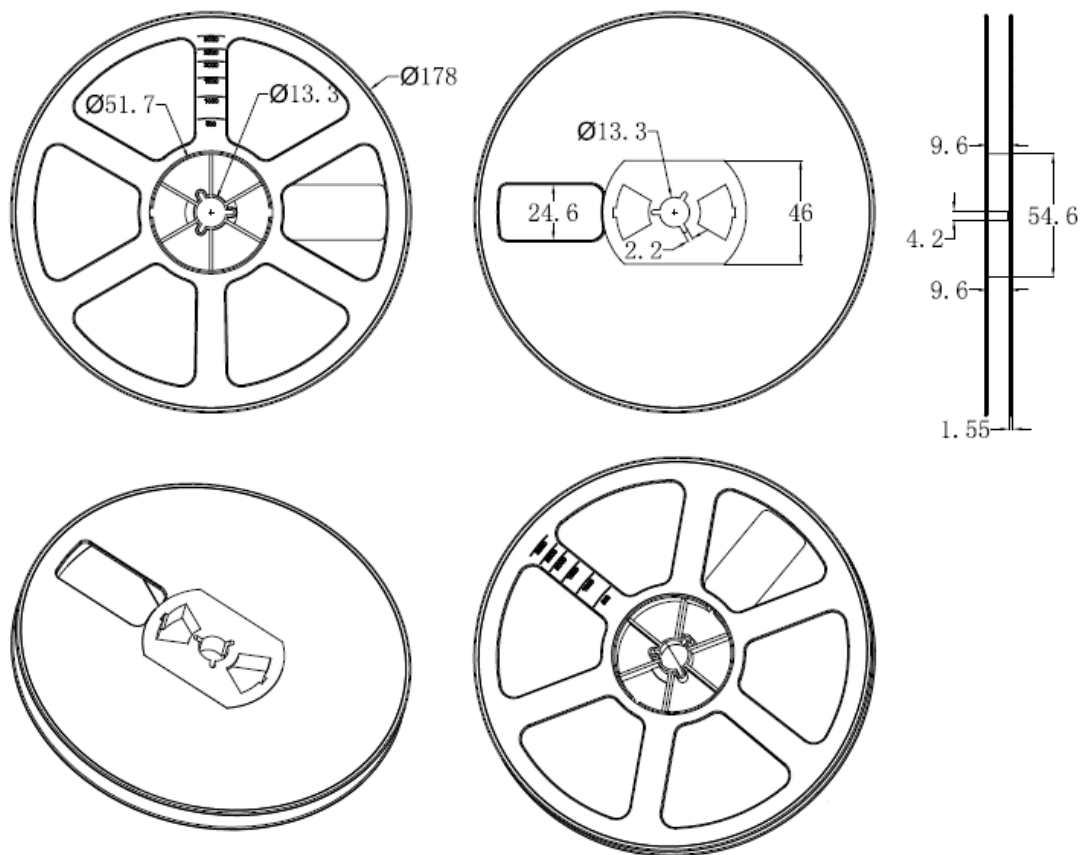




Symbol	A0	A1	B0	B1	K0	D <sub>0</sub>	D <sub>1</sub>	P <sub>0</sub>	P <sub>1</sub>
Spec	3.15±0.10	1.15±0.10	2.80±0.10	2.15±0.10	1.30±0.10	1.55±0.10	1.10±0.10	4.00±0.10	4.00±0.10
Symbol	W	E	F	P <sub>2</sub>	t	t1	10*P0	4-P0	
Spec	7.95±0.05	1.70±0.05	3.50±0.10	2.00±0.10	0.21±0.02	0.05以上	40.00±0.10	4.00±0.10	

NOTE:

- 1.材料: PC+PS导电
- 2.10个链孔的累积公差不能超过0.2MM;
- 3.250MM带子的扇形不得超过1MM;
- 4.按照EIA-481-D的要求。





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