SSC8037GQ4

P-Channel Enhancement Mode MOSFET

➢ Features

VDS	VGS	RDSON Typ.	ID
-30V	±25V	14mR@-10V	-42A
		23mR@-4V5	

➢ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage power management requiring a wild range of given voltage ratings(4.5V~18V) such as load switch and battery protection.

➢ Applications

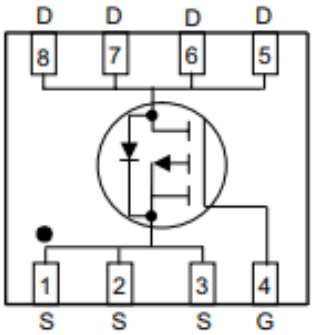
- Load Switch
- NB battery
- DCDC conversion

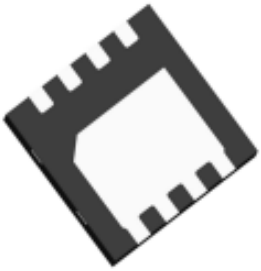
➢ Ordering Information

Device	Package	Shipping
SSC8037GQ4	DFN3x3	5000/Reel

➢ Pin configuration

Top view





Bottom View

(Y: year/W: week)

Marking

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V_{DSS}	Drain-to-Source Voltage		-30	V
V_{GSS}	Gate-to-Source Voltage		±25	V
I_D	Continuous Drain Current	TC=25℃	-42	A
		TC=100℃	-22	
I_{DSM}	Continuous Drain Current [a]	TA=25℃	-12	A
		TA=70℃	-8.5	
I_{DM}	Pulsed Drain Current [b]		-168	A
I_{AS}	Avalanche Current[b] L=0.5mH		21	A
E_{AS}	Avalanche Energy[b] L=0.5mH		110	mJ
P_D	Power Dissipation [c]	TC=25℃	40	W
		TC=100℃	16	W
P_{DSM}	Power Dissipation [a]	TA=25℃	3.2	W
		TA=70℃	2.1	W
T_J	Operation junction temperature		-55 to 150	℃
T_{STG}	Storage temperature range		-55 to 150	

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	38.8	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	3.1	

Note:

a. The value of RθJA is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with TA=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

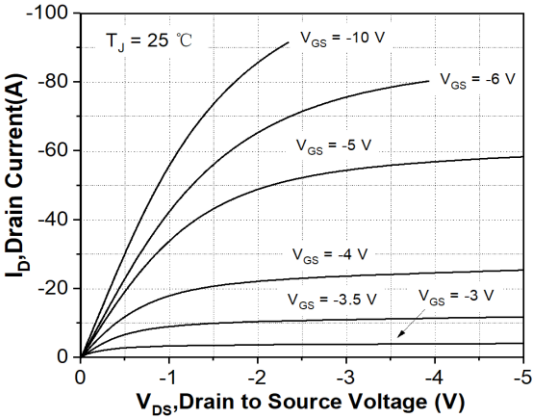
b. Repetitive rating, pulse width limited by junction temperature.

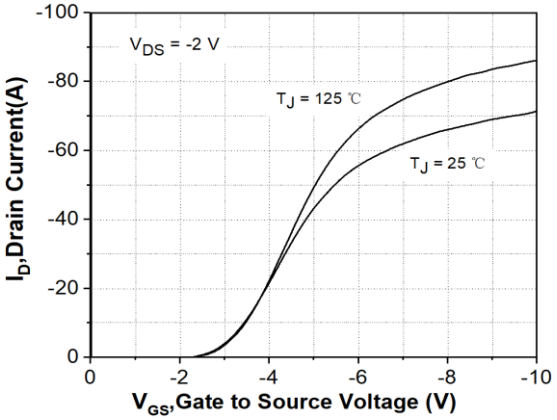
c. The power dissipation PD is based on TJ(MAX)=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

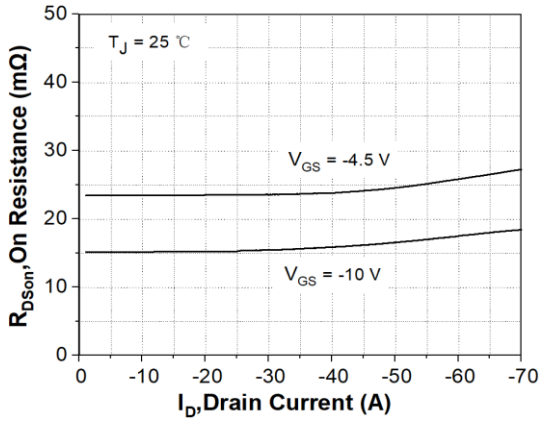
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

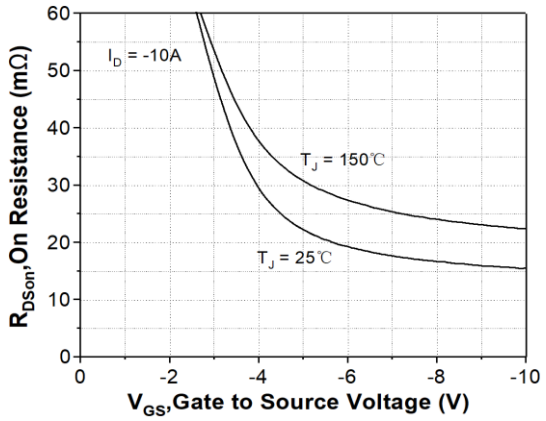
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V , ID=-250uA	-30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS , ID=-250uA	-1	-1.8	-3	V
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=-10V , ID=-10A		14	19	mR
		VGS=-4.5V , ID=-8A		23	30	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=-30V , VGS=0V			-1	uA
I_{GSS}	Gate-Source leak current	VGS=±25V , VDS=0V			±100	nA
G_{FS}	Transconductance	VDS=-5V , ID=-10A		16		S
V_{SD}	Forward Voltage	VGS=0V , IS=-5A		-0.85	-1.3	V
Ciss	Input Capacitance	VDS=-15V , VGS=0V, f=1MHz		1300		pF
Coss	Output Capacitance			161		
Crss	Reverse Transfer Capacitance			183		
Q_G	Total Gate charge	VGS=-10V , VDS=-15V, ID=-10A		25.5		nC
Q_{GS}	Gate to Source charge			4.3		
Q_{GD}	Gate to Drain charge			6.1		
$T_{D(ON)}$	Turn-on delay time	VGS=-10V, VDS=-15V, RL=3R, RG=1R		8		ns
Tr	Rise time			33.5		
$T_{D(OFF)}$	Turn-off delay time			48		
Tf	Fall time			11		
Trr	Diode Recovery Time	IF=-10A, di/dt=200A/us		23		ns
Qrr	Diode Recovery Charge			8		nC

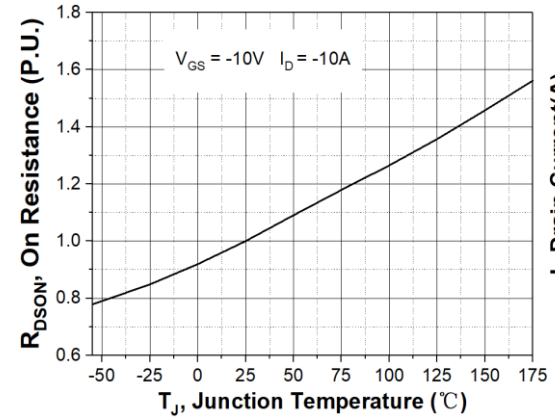
➢ **Typical Characteristics**(T_A=25℃ unless otherwise noted)

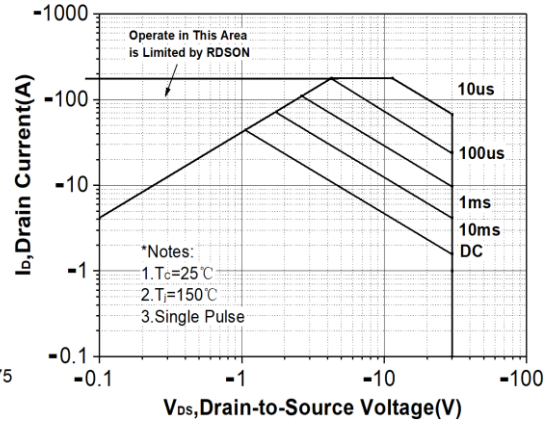


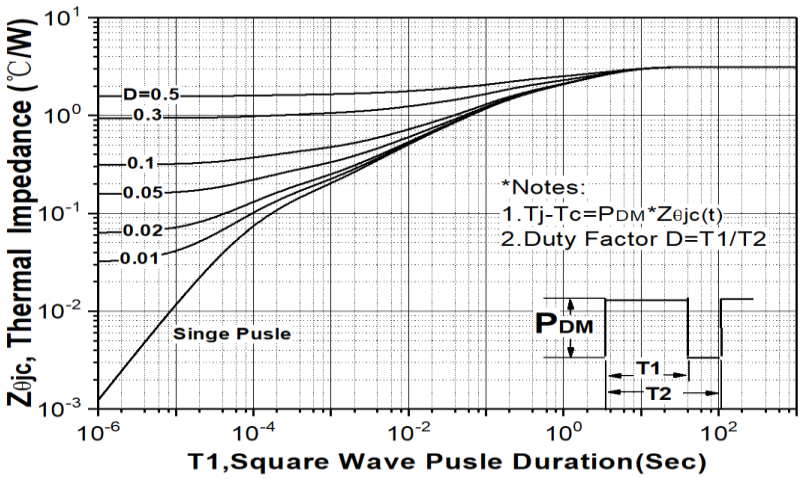




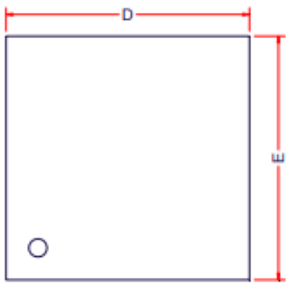




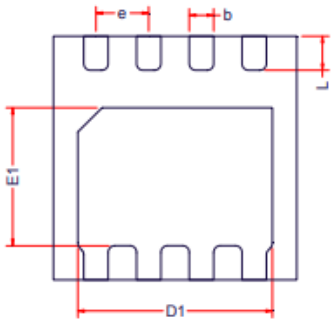




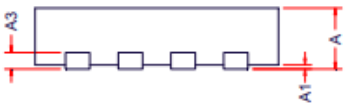
➢ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.20Ref	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
b	0.25	0.30	0.35
e		0.65BSC	
L	0.37	0.42	0.47

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