



# SSC8137GSB

## P-Channel Enhancement Mode MOSFET

### ➤ Features

VDS	VGS	RDS(on) Typ.	ID
-30V	±20V	23mR@-10V	-7A
		31mR@-4V5	

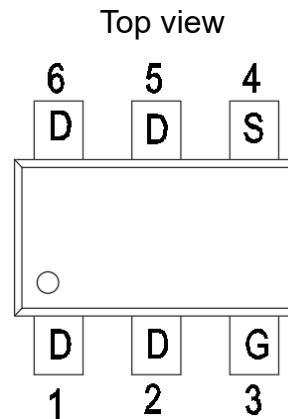
### ➤ Description

This P-Channel enhancement mode power FETs are produced with high cell density, DMOS trench technology, which is especially used to minimize on-state resistance. This device is particularly suited for low voltage application such as portable equipment, power management and other battery powered circuits and low in-line power loss are needed in a very small outline surface mount package.

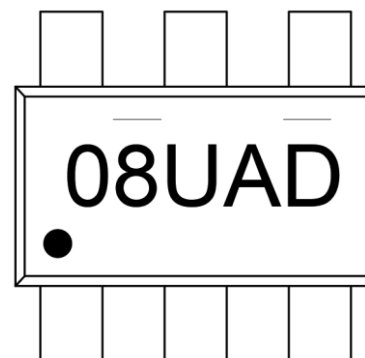
### ➤ Applications

- TFT panel power switch
- High side DC/DC Converter
- High side driver for brushless DC motor
- Portable DVD, DPF

### ➤ Pin configuration



SOT23-6L



Marking

### ➤ Ordering Information

Device	Package	Shipping
SSC8137GSB	SOT23-6	3000/Reel



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	-30	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>a</sup>	-7	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	-28	A
$P_D$	Power Dissipation <sup>a</sup>	2	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>	64	$^{\circ}\text{C}/\text{W}$

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.

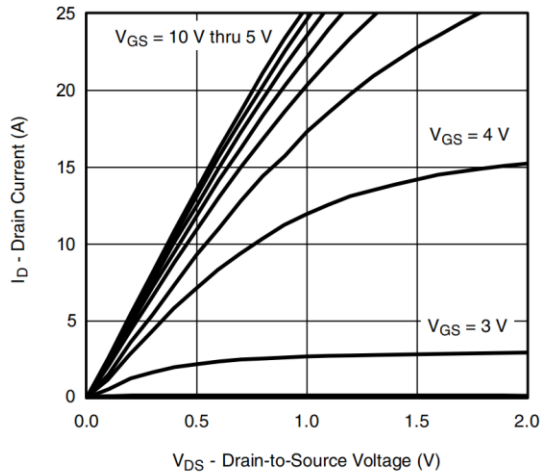


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

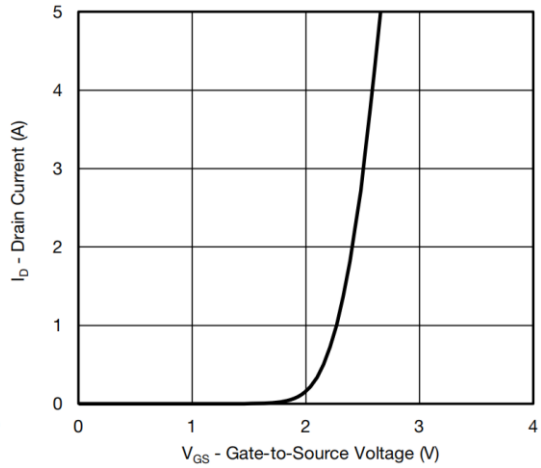
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-5A$		23	30	mR
		$V_{GS}=-4.5V, I_D=-4A$		31	45	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-30V, V_{GS}=0V$			-1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=-10V, I_D=-5A$		15		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=-3A$		-0.8	-1.3	V
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, F=1\text{MHz}$		1400		pF
$C_{oss}$	Output Capacitance			730		
$C_{rss}$	Reverse Transfer Capacitance			590		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-10V, V_{DS}=-15V, R_L=2R, R_G=3R, I_D=-2A$		11		ns
$T_r$	Rise time			25		
$T_{D(OFF)}$	Turn-off delay time			70		
$T_f$	Fall time			41		
$Q_G$	Total Gate Charge	$V_{GS}=-10V, V_{DS}=-15V, I_D=-2A$		25		nC
$Q_{GS}$	Gate to Source Charge			2		
$Q_{GD}$	Gate to Drain Charge			4		



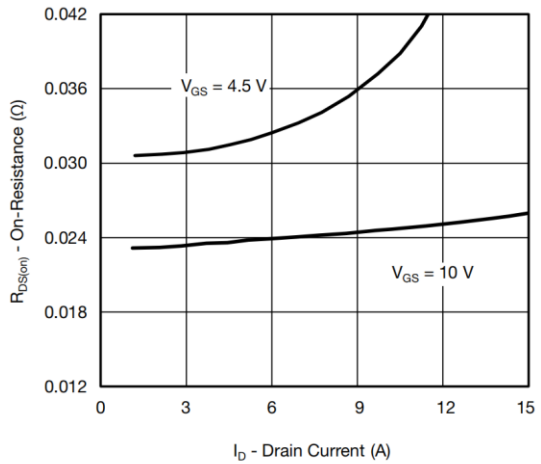
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)



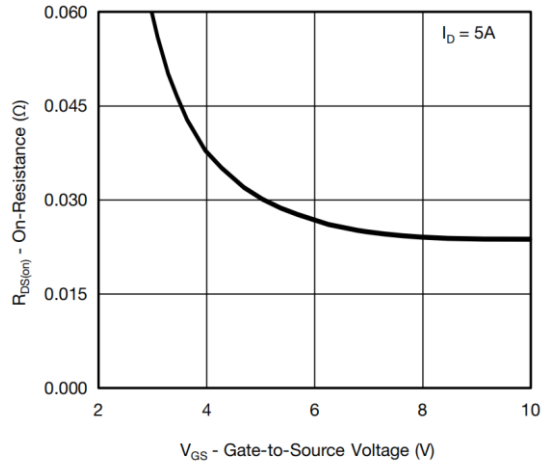
**Output Characteristics**



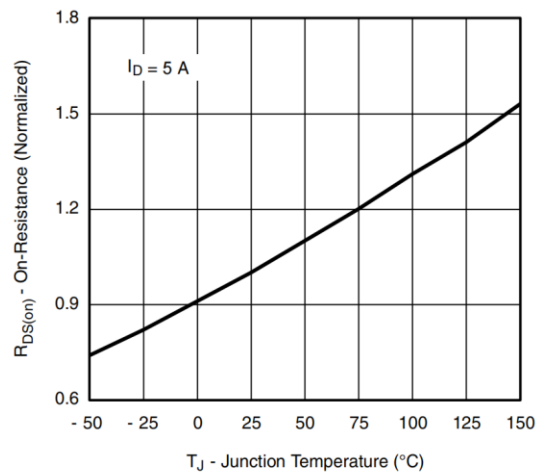
**Transfer Characteristics**



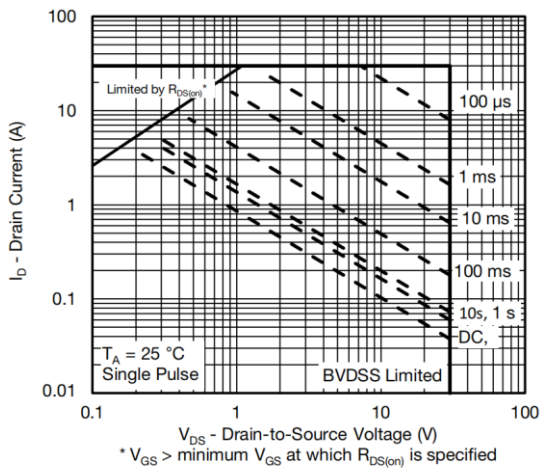
**On-Resistance vs. Drain Current**



**On-Resistance vs. Gate-to-Source Voltage**



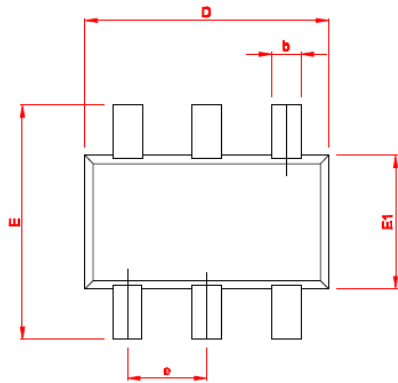
**On-Resistance vs. Junction Temperature**



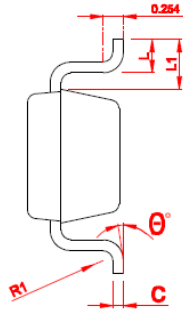
**Safe Operating Area**



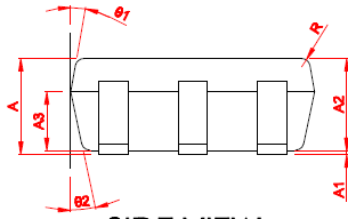
➤ Package Information



TOP VIEW



SIDE VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* $\theta$	0	--	8°
$\theta_1$	8°	10°	12°
$\theta_2$	10°	12°	14°

SOT23-6L



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