

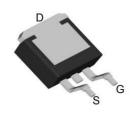
SSC8239GT6

P-Channel Enhancement Mode MOSFET

Features

V _{DS}	V _{GS}	R _{DS(ON)}	l _D
-30V	±20V	6.5mΩ@-10V	-84A
-30 V	<u> </u>	8.9mΩ@-4V5	-04/

Pin configuration

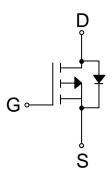


TO-263-3L (Bottom View)

> Description

This SSC8239GT6 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

100% UIS + ΔVDS + Rg Tested!



Pin Configuration

Applications

- Load Switch
- NB Battery
- DCDC Conversion

8239YW

Marking

(YW: Internal Traceability Code)

Ordering Information

Device	Package	Shipping
SSC8239GT6	TO-263-3L	1000/Box



➤ Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit	
V_{DSS}	Drain-to-Source Volta	Drain-to-Source Voltage		V	
V_{GSS}	Gate-to-Source Volta	Gate-to-Source Voltage		V	
	Continuous Dunin Comment d	T _C =25°C	-84	^	
l _D	Continuous Drain Current d	T _C =100°C	-47	Α	
	Overtice on Basic Overest S	T _A =25℃	-17	^	
IDSM	Continuous Drain Current ^a	T _A =70°C	-12	A	
I _{DM}	Pulsed Drain Curren	Pulsed Drain Current b		Α	
L	D Discipation 0	Tc=25°C	74	10/	
P _D	Power Dissipation ^c	T _C =100°C	29	W	
D.	Danna Diagination 2	T _A =25℃	2.9	107	
P _{DSM}	Power Dissipation ^a	wer Dissipation a T _A =70℃	1.9	W	
I _{AS}	Avalanche Current b L=0.5mH \$	Avalanche Current b L=0.5mH Single Pulse		Α	
Eas	Avalanche Energy b L=0.5mH Single Pulse		225	mJ	
TJ	Operation junction tempe			*0	
T _{STG}	Storage temperature ra	ange	-55~150	$^{\circ}$	

➤ Thermal Resistance Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance a	43	°C/W
R _{θJC}	Junction-to-Case Thermal Resistance	1.7	C/VV

Note:

- a. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with T_A=25 °C. The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P_D is based on $T_{J(MAX)}$ =150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.

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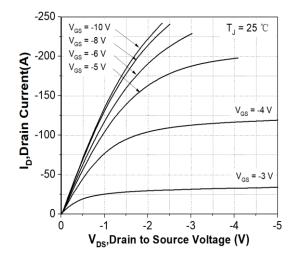


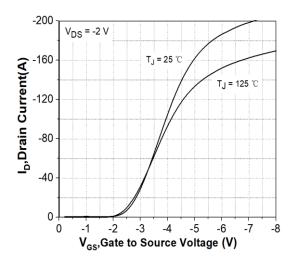
\succ Electrical Characteristics (T_A=25°C unless otherwise noted)

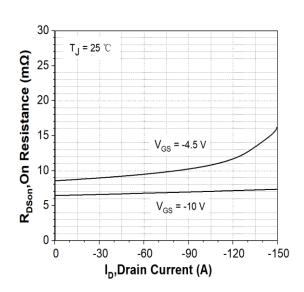
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0V, I_{D} = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250uA$	-1	-1.5	-2.5	V
Drain Course On Registeres	Б	V _{GS} = -10V, I _D = -20A		6.5	8.5	0
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -4.5V, I _D = -10A		8.9	12	mΩ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			1	μA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0V			±100	nA
Transconductance	G _{FS}	V _{DS} = -5V, I _D = -10A		35		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = -5A		-0.8	-1.3	V
Gate Resistance	R _G	V _{DS} = 0V, f = 1MHz		2.3		Ω
Input Capacitance	Ciss	\/ 45\/\\ 0\/		4900		
Output Capacitance	Coss	V _{DS} = -15V, V _{GS} = 0V,		520		pF
Reverse Transfer Capacitance	Crss	T = TIVIMZ		400		
Total Gate Charge	Q _G	f = 1MHz V _{GS} = -10V, V _{DS} = -15V, I _D = -20A		82		
Gate to Source Charge	Q _{GS}			11		nC
Gate to Drain Charge	Q _{GD}	ID = -20A		20		
Turn-on Delay Time	T _{D(ON)}			16		
Rise Time	Tr	V _{GS} = -10V, V _{DS} = -15V,		52		
Turn-off Delay Time	T _{D(OFF)}	$R_L=0.75\Omega,R_G=3\Omega$		107		ns
Fall Time	T _f			26		
Diode Recovery Time	Trr	I _F =-20A, di/dt=500A/us		26		ns
Diode Recovery Charge	Q _{rr}	I _F =-20A, di/dt=500A/us		18		nC

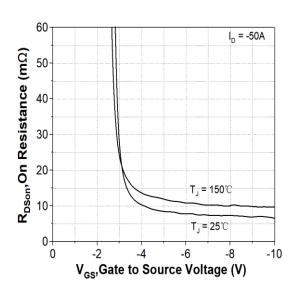


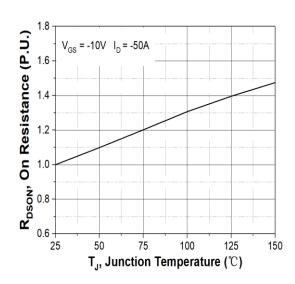
> Typical Performance Characteristics (T_A=25℃ unless otherwise noted)

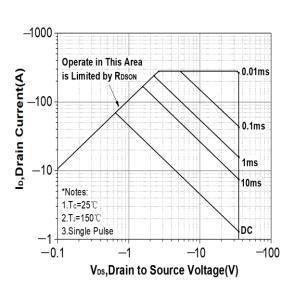






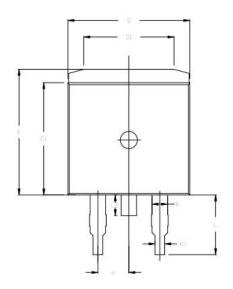






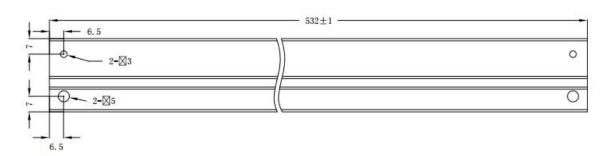


Package Information

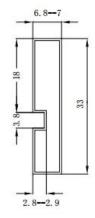




SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
А	4,40		4.60	
b	1.20		1.36	
k1	0.70		0.90	
C	0.48		0.53	
C1	1.28		1.32	
CS	0.04	0.12	0.20	
D	9.80	10.00	10.20	
D1	7.25	7.40	7.55	
E	10.20	10.30	10.40	
E1	9.10	9.20	9,30	
е		2.54	1-1-1	
L	4.70	4.90	5.10	
1.1	2,40	2.60	2.80	
T5	1.50	1.70	1.90	



 $T=0.5 \pm 0.1$



- 技术要求: 1. 材料: 透明PVC
- 2. 表面电阻: 10E5~10E10 0HMS/SQ 3. 未注尺寸公差±0.3 4. 黑色钉子由厂家出货时塞于左端



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