SSC8624GSB

N- and P-Channel Complementary, MOSFET

➢ Features

N-Channel

VDS	VGS	RDSON Typ.	ID	ESD
20V	±8V	380mR@4V5	1A	1.2KV
		450mR@2V5		
		600mR@1V8		

P-Channel

VDS	VGS	RDSON Typ.	ID
-20V	±12V	220mR@-4V5	-1A
		260mR@-2V5	
		330mR@-1V8	

➢ Description

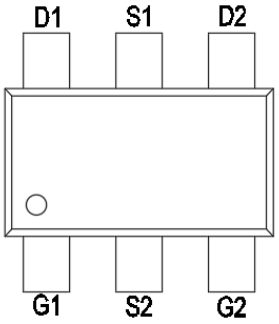
SSC8624GSB uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

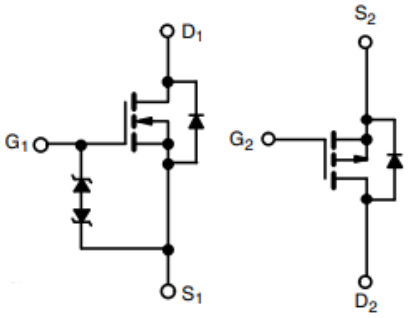
➢ Applications

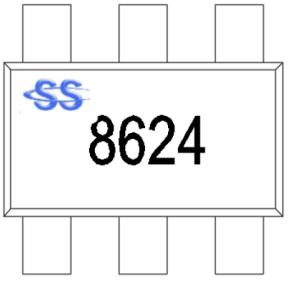
- Signal
- CCFL Driver

➢ Pin configuration

Top view







Marking

➢ Ordering Information

Device	Package	Shipping
SSC8624GSB	SOT23-6L	3000/Reel

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	N-Channel	P-Channel	Unit
V_{DSS}	Drain-to-Source Voltage	20	-20	V
V_{GSS}	Gate-to-Source Voltage	±8	±12	V
I_D	Continuous Drain Current [a]	1	-1	A
I_{DM}	Pulsed Drain Current [b]	3	-3	A
P_{DSM}	Power Dissipation [a]	1		W
P_D	Power Dissipation [c]	0.4		W
T_J	Operation junction temperature	-55 to 150		℃
T_{STG}	Storage temperature range	-55 to 150		℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		315	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		125	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

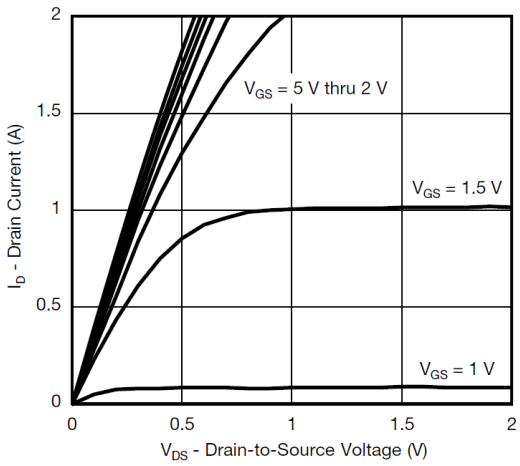
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

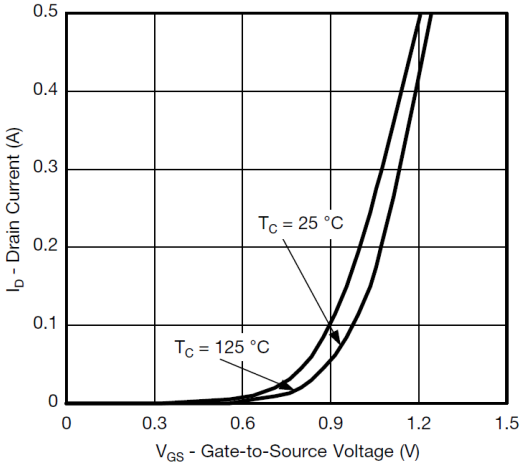
Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	N-CH	20			V
		VGS=0V,ID=-250uA	P-CH	-20			
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	N-CH	0.4	0.9	1.2	V
		VDS=VGS,ID=-250uA	P-CH	-0.4	-0.7	-1	
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=4.5V, ID=1A	N-CH		380	550	mR
		VGS=-4.5V, ID=-1A	P-CH		220	300	
		VGS=2.5V, ID=0.5A	N-CH		450	700	
		VGS=-2.5V, ID=-0.5A	P-CH		260	450	
		VGS=1.8V, ID=0.5A	N-CH		600	1000	
		VGS=-1.8V, ID=-0.5A	P-CH		330	600	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=16V, VGS=0V	N-CH			1	uA
		VDS=-16V,VGS=0V	P-CH			-1	
I_{GSS}	Gate-Source leak current	VGS=±8V,VDS=0V	N-CH			±10	uA
		VGS=±12V,VDS=0V	P-CH			±100	nA
G_{FS}	Forward Transconductance	VDS=5V, ID=1A	N-CH		1		S
		VDS=-5V, ID=-1A	P-CH		2		
V_{SD}	Forward Voltage	VGS=0V,IS=0.5A	N-CH		0.7	1.3	V
		VGS=0V,IS=-0.5A	P-CH		-0.7	-1.3	
Ciss	Input Capacitance	**NMOS:** VDS=10V, VGS=0V, f=1MHZ **PMOS:** VDS=-10V, VGS=0V, f=1MHZ	N-CH		40		pF
			P-CH		160		
Coss	Output Capacitance		N-CH		10		
			P-CH		33		
Crss	Reverse Transfer Capacitance		N-CH		4		
			P-CH		10		

Qg	Total Gate Charge	**NMOS:** VDS=10V, VGS=4.5V, ID=1A **PMOS:** VDS=-10V, VGS=-4.5V, ID=-1A	N-CH		0.6		nC
			P-CH		1.6		
Qgs	Gate Source Charge		N-CH		0.2		
			P-CH		0.4		
Qgd	Gate Drain Charge		N-CH		0.2		
			P-CH		0.3		
$T_{D(ON)}$	Turn-on delay time	**NMOS:** VDS=10V, VGS=4.5V, RL=10R, RG=1R **PMOS:** VDS=-10V, VGS=-4.5V, RL=10R, RG=1R	N-CH		2		ns
			P-CH		5		
Tr	Rise time		N-CH		14		
			P-CH		10		
$T_{D(OFF)}$	Turn-off delay time		N-CH		11		
			P-CH		10		
Tf	Fall time		N-CH		7		
			P-CH		8		

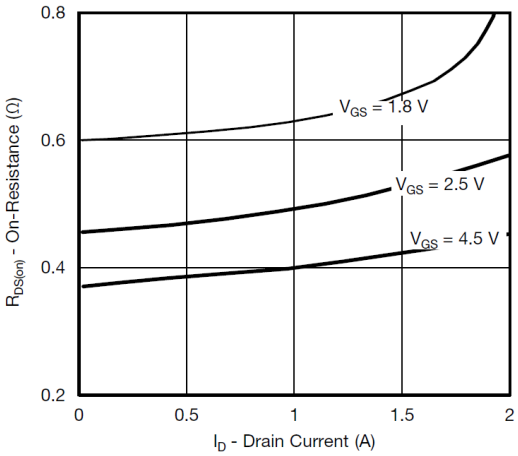
➢ N-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)



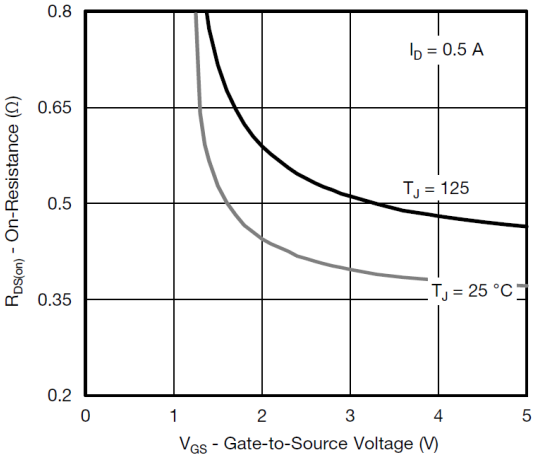
Output Characteristics



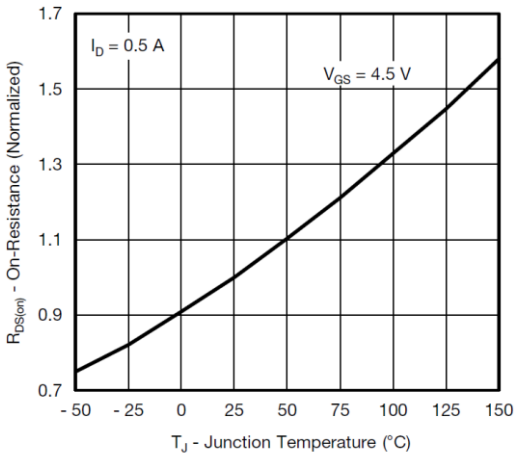
Transfer Characteristics



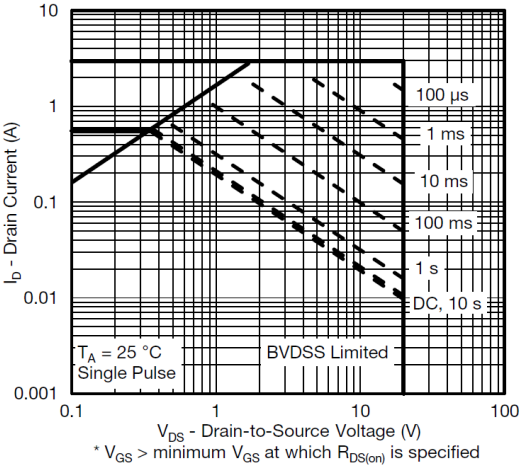
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage

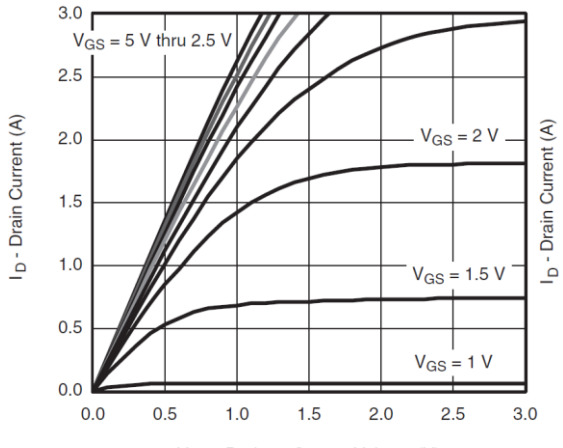


On-Resistance vs. Junction Temperature

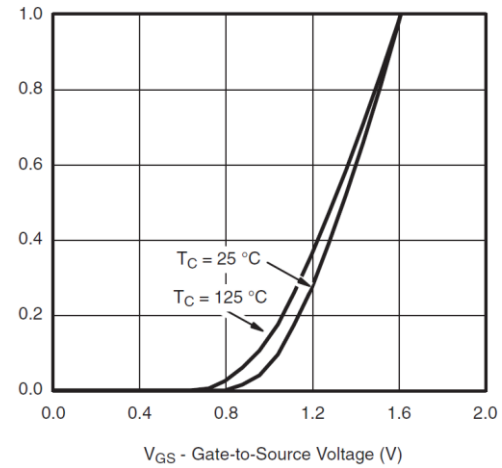


Safe Operating Area, Junction-to-Ambient

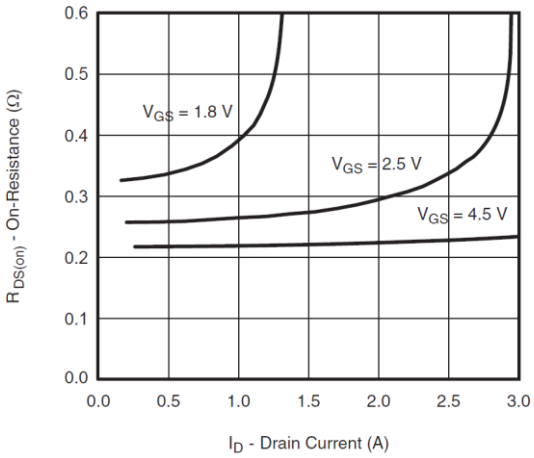
➢ P-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)



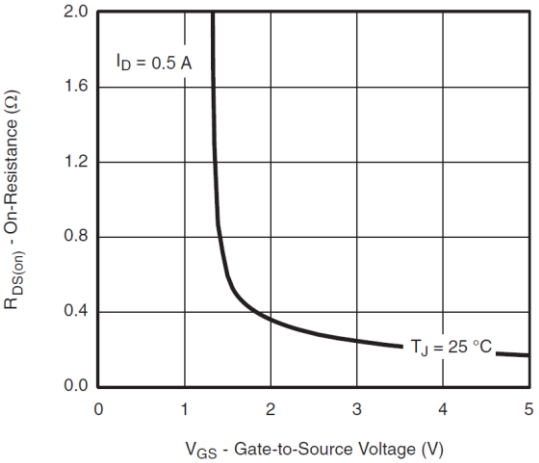
Output Characteristics



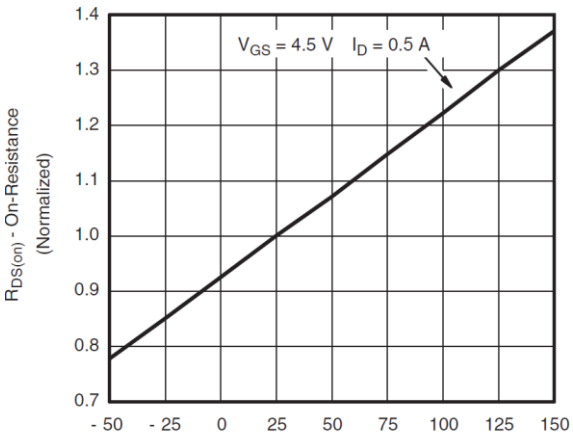
Transfer Characteristics



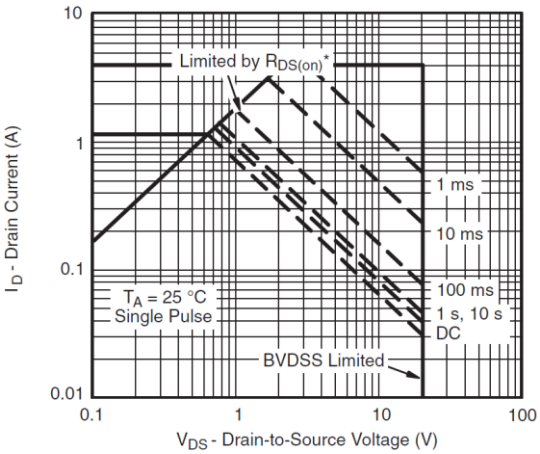
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage



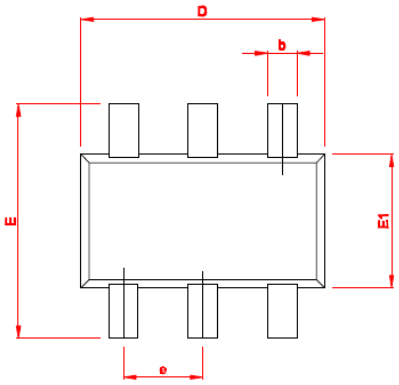
On-Resistance vs. Junction Temperature

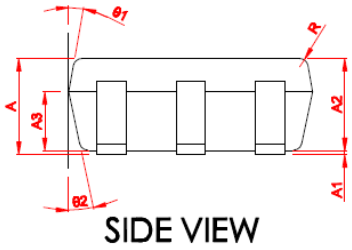


* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

➢ Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* θ	0	--	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

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