SSC8626GN2

N- and P-Channel Complementary, MOSFET

➢ Features

N-Channel

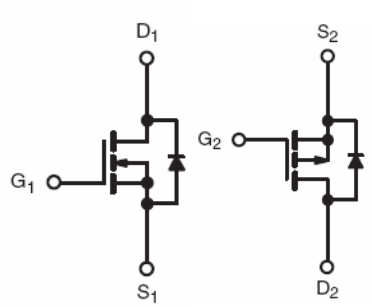
VDS	VGS	RDSON Typ.	ID
20V	±12V	22mR@4V5	7A
		27mR@2V5	
		36mR@1V8	

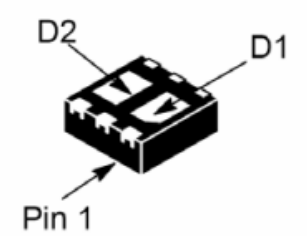
P-Channel

VDS	VGS	RDSON Typ.	ID
-20V	±12V	63mR@-4V5	-4A
		87mR@-2V5	
		120mR@-1V8	

➢ Pin configuration

Top view





DFN2020

➢ Description

SSC8626GN2 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

Marking

➢ Applications

- Signal
- CCFL Driver

➢ Ordering Information

Device	Package	Shipping
SSC8626GN2	DFN2020	3000/Reel

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	N	P	Unit
V_{DSS}	Drain-to-Source Voltage	20	-20	V
V_{GSS}	Gate-to-Source Voltage	±12	±12	V
I_D	Continuous Drain Current [a]	7	-4	A
I_{DM}	Pulsed Drain Current [b]	21	-12	A
P_D	Power Dissipation [c]	1.9	1.9	W
TJ	Operation junction temperature	-55 to 150		℃
TSTG	Storage temperature range	-55 to 150		℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Ratings		Unit
		N	P	
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]	65	65	℃/W

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design.

b. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

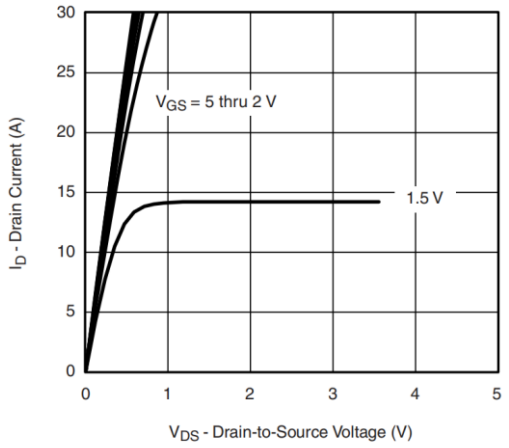
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using steady state junction-to-ambient thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

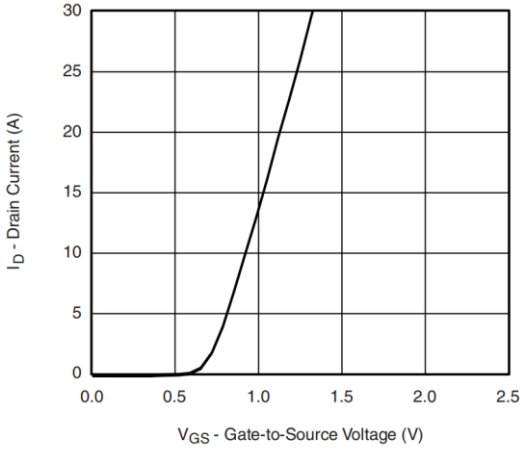
Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	N-CH	20			V
		VGS=0V,ID=-250uA	P-CH	-20			
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	N-CH	0.4	0.6	0.9	V
		VDS=VGS,ID=-250uA	P-CH	-0.5	-0.7	-1.2	
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=4.5V, ID=5A	N-CH		22	26	mR
		VGS=-4.5V, ID=-2.8A	P-CH		63	80	
		VGS=2.5V, ID=3.5A	N-CH		27	35	
		VGS=-2.5V, ID=-2.3A	P-CH		87	110	
		VGS=1.8V, ID=2.8A	N-CH		36	55	
		VGS=-1.8V, ID=-0.5A	P-CH		120	200	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=16V, VGS=0V	N-CH			1	uA
		VDS=-16V,VGS=0V	P-CH			-1	
I_{GSS}	Gate-Source leak current	VGS=±12V,VDS=0V	N-CH			±100	nA
		VGS=±12V,VDS=0V	P-CH			±100	nA
G_{FS}	Forward Transconductance	VDS=5V, ID=7A	N-CH		7		S
		VDS=-5V, ID=-4A	P-CH		4		
V_{SD}	Forward Voltage	VGS=0V,IS=1.1A	N-CH		0.8	1.3	V
		VGS=0V,IS=-0.9A	P-CH		-0.7	-1.3	
Ciss	Input Capacitance	**NMOS:** VDS=10V, VGS=0V, f=1MHZ **PMOS:** VDS=-10V, VGS=0V, f=1MHZ	N-CH		406		pF
			P-CH		730		
Coss	Output Capacitance		N-CH		68		
			P-CH		72		
Crss	Reverse Transfer Capacitance		N-CH		57		
			P-CH		60		

Qg	Total Gate Charge	**NMOS:** VDS=10V, VGS=4.5V, ID=7A **PMOS:** VDS=-10V, VGS=-4.5V, ID=-4A	N-CH		11		nC
			P-CH		8		
Qgs	Gate Source Charge		N-CH		1		
			P-CH		1		
Qgd	Gate Drain Charge		N-CH		1.5		
			P-CH		2		
$T_{D(ON)}$	Turn-on delay time	**NMOS:** VGS=4.5V, VDS=10V, RG=3R,ID=7A **PMOS:** VGS=-4.5V, VDS=-10V, RG=3R,ID=-4A	N-CH		3		ns
			P-CH		12		
Tr	Rise time		N-CH		7.5		
			P-CH		11		
$T_{D(OFF)}$	Turn-off delay time		N-CH		20		
			P-CH		40		
Tf	Fall time		N-CH		6		
			P-CH		17		

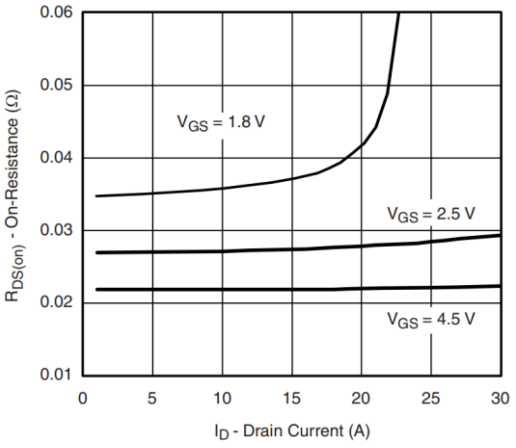
➢ N-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)



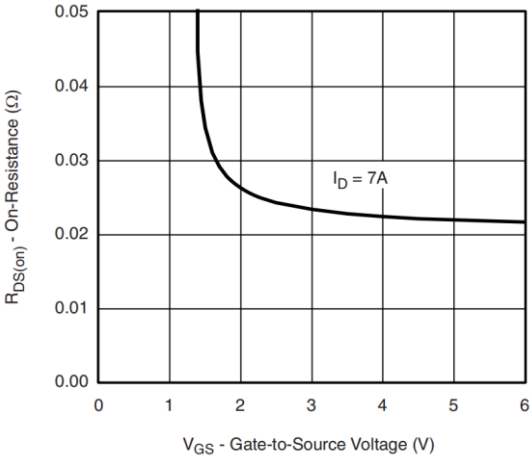
Output Characteristics



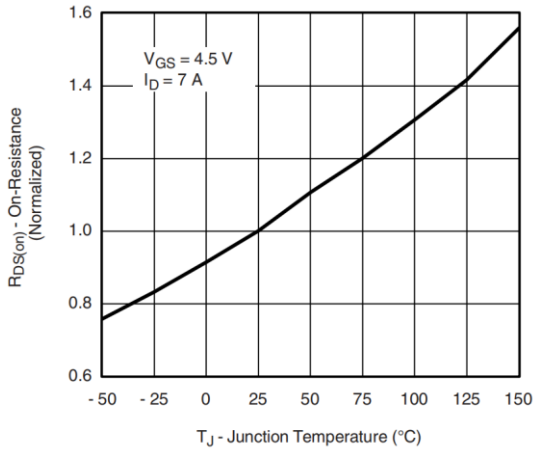
Transfer Characteristics



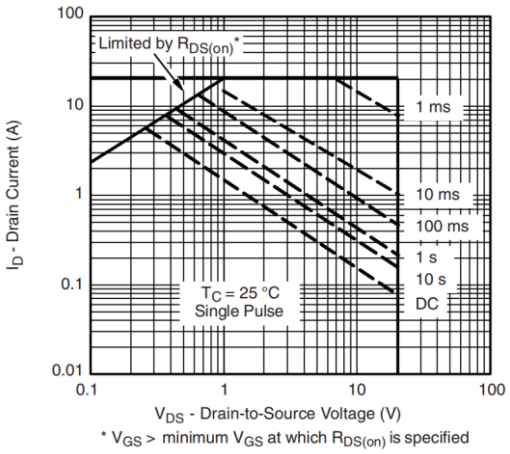
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage

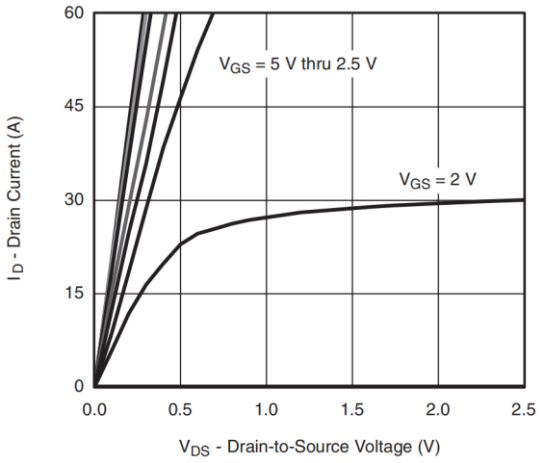


On-Resistance vs. Junction Temperature

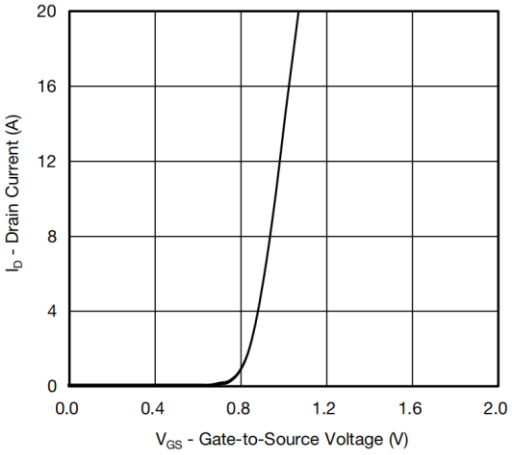


Safe Operating Area, Junction-to-Case

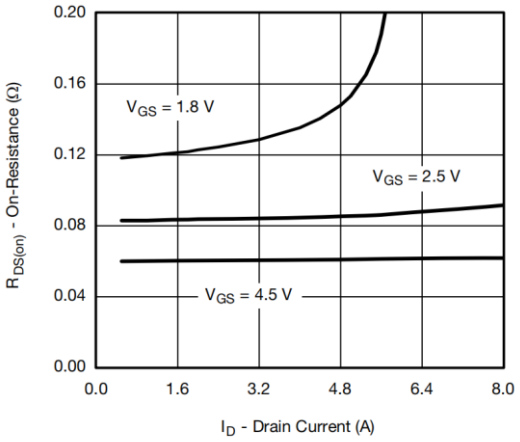
➢ P-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)



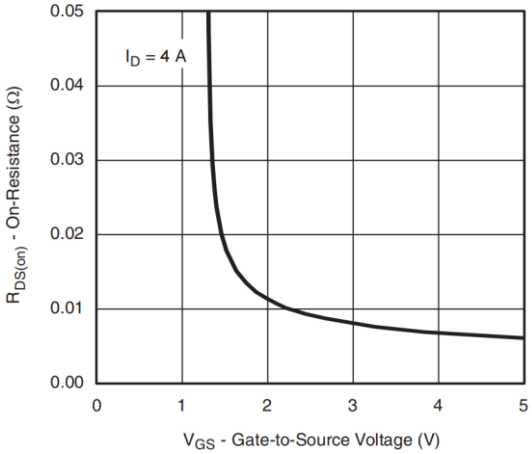
Output Characteristics



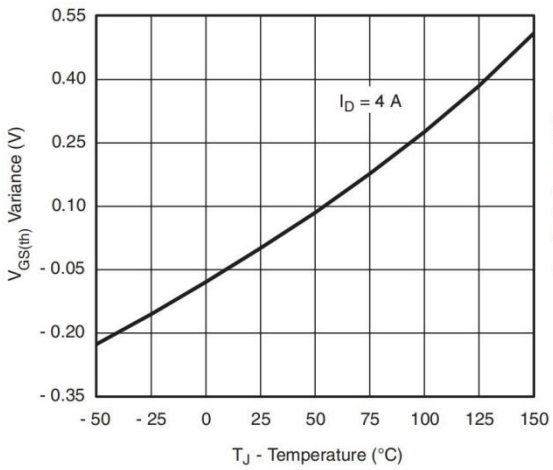
Transfer Characteristics



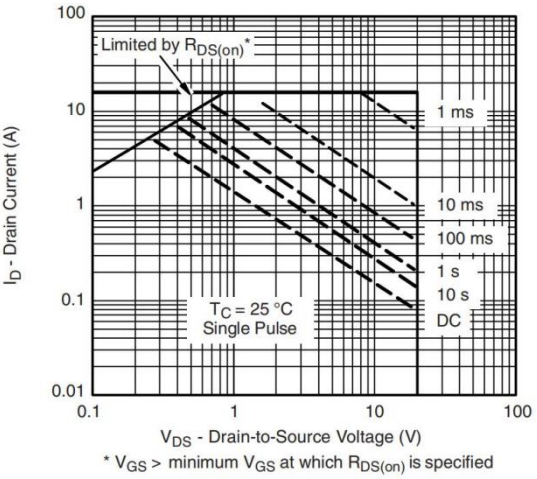
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage



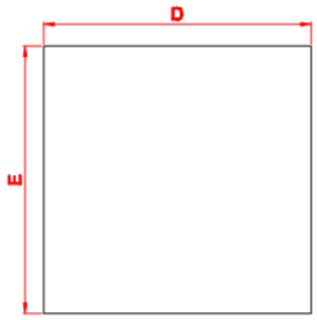
Threshold Voltage



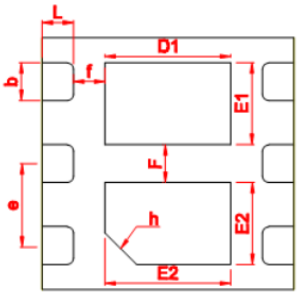
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

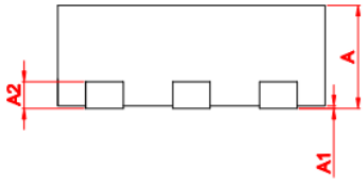
➢ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
* A1	0.000	0.020	0.050
* b	0.275	0.300	0.325
* A2	0.190	0.210	0.230
* D	1.900	2.000	2.100
* E	1.900	2.000	2.100
* E1	0.570	0.620	0.670
* E2	0.570	0.620	0.670
* D1	0.950	1.000	1.050
* D2	0.950	1.000	1.050
* e	0.600	0.650	0.700
h	0.300	0.350	0.400
* L	0.200	0.250	0.300
* F	0.250	0.300	0.350
* f	0.200	0.250	0.300

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